

FIG. 1

PRIOR ART

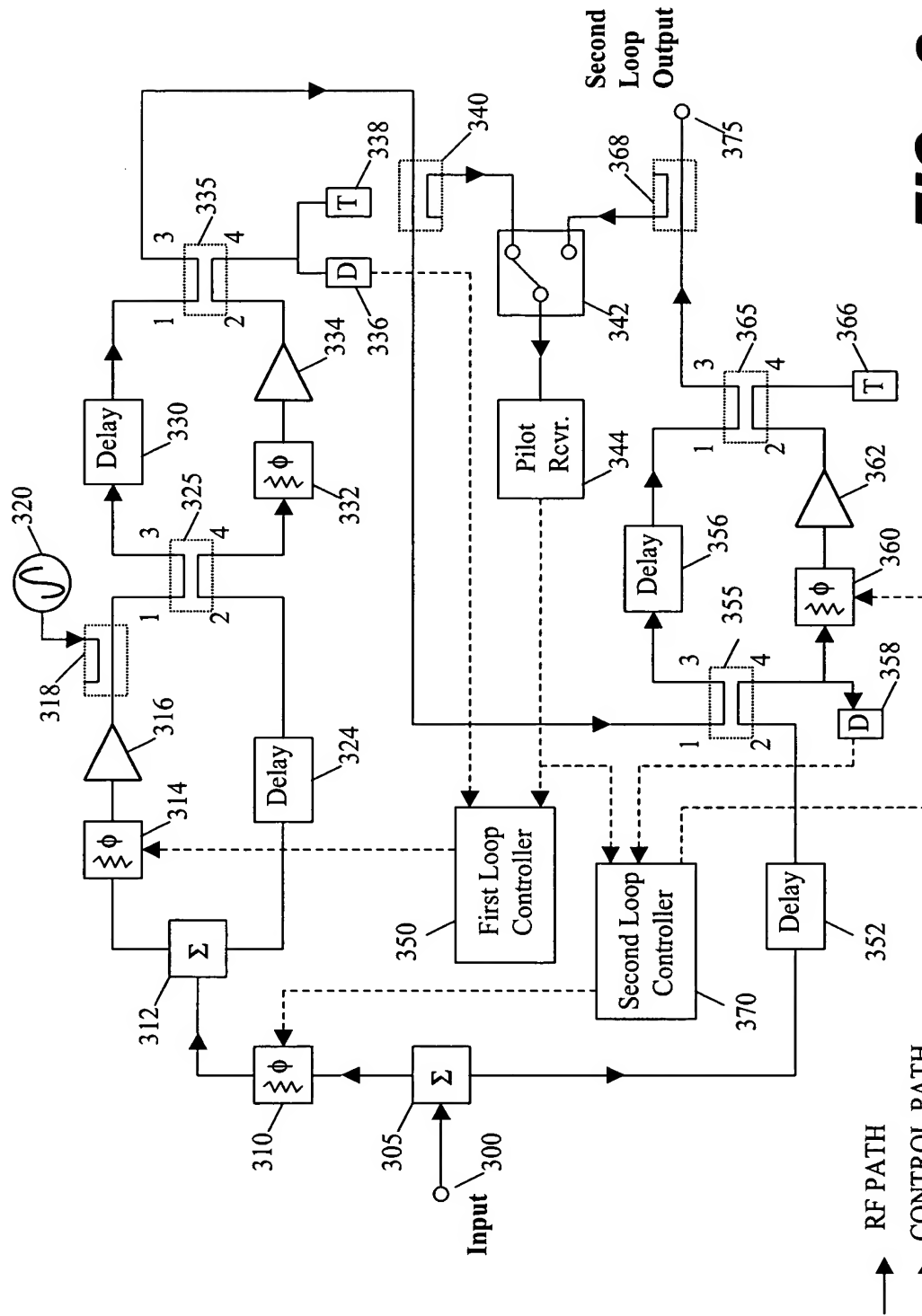


FIG. 2

PRIOR ART

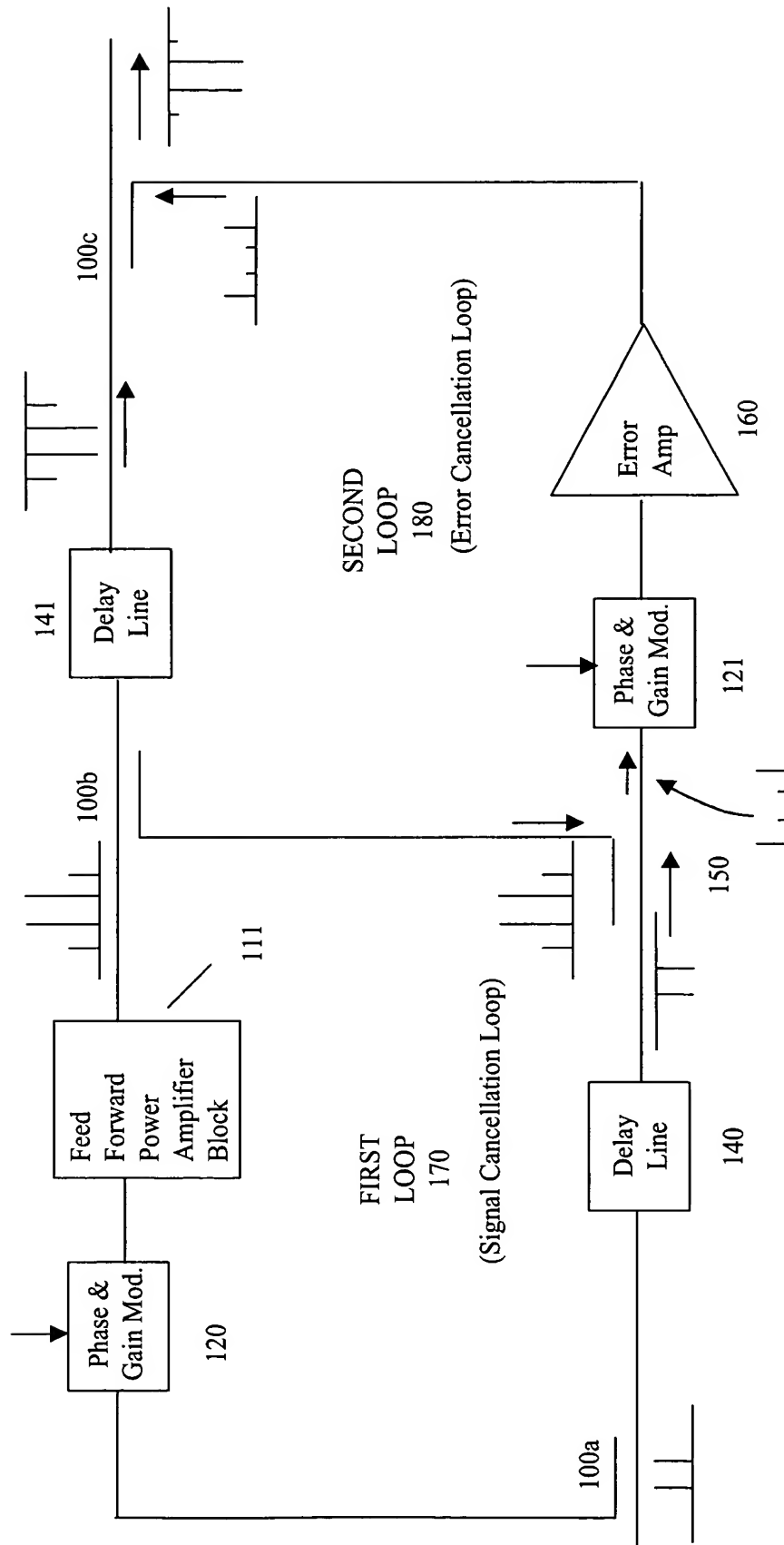
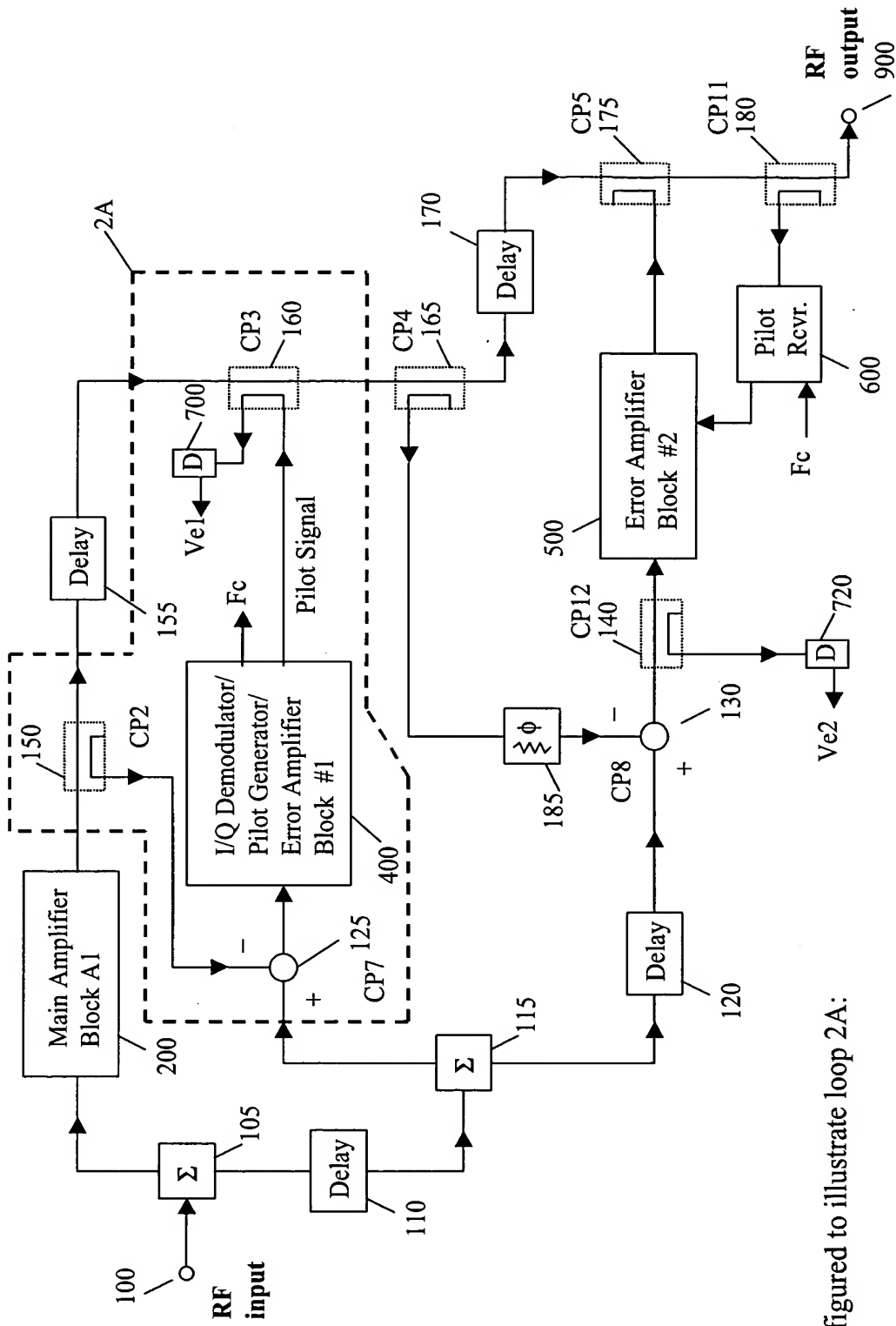


FIG. 3

PRIOR ART

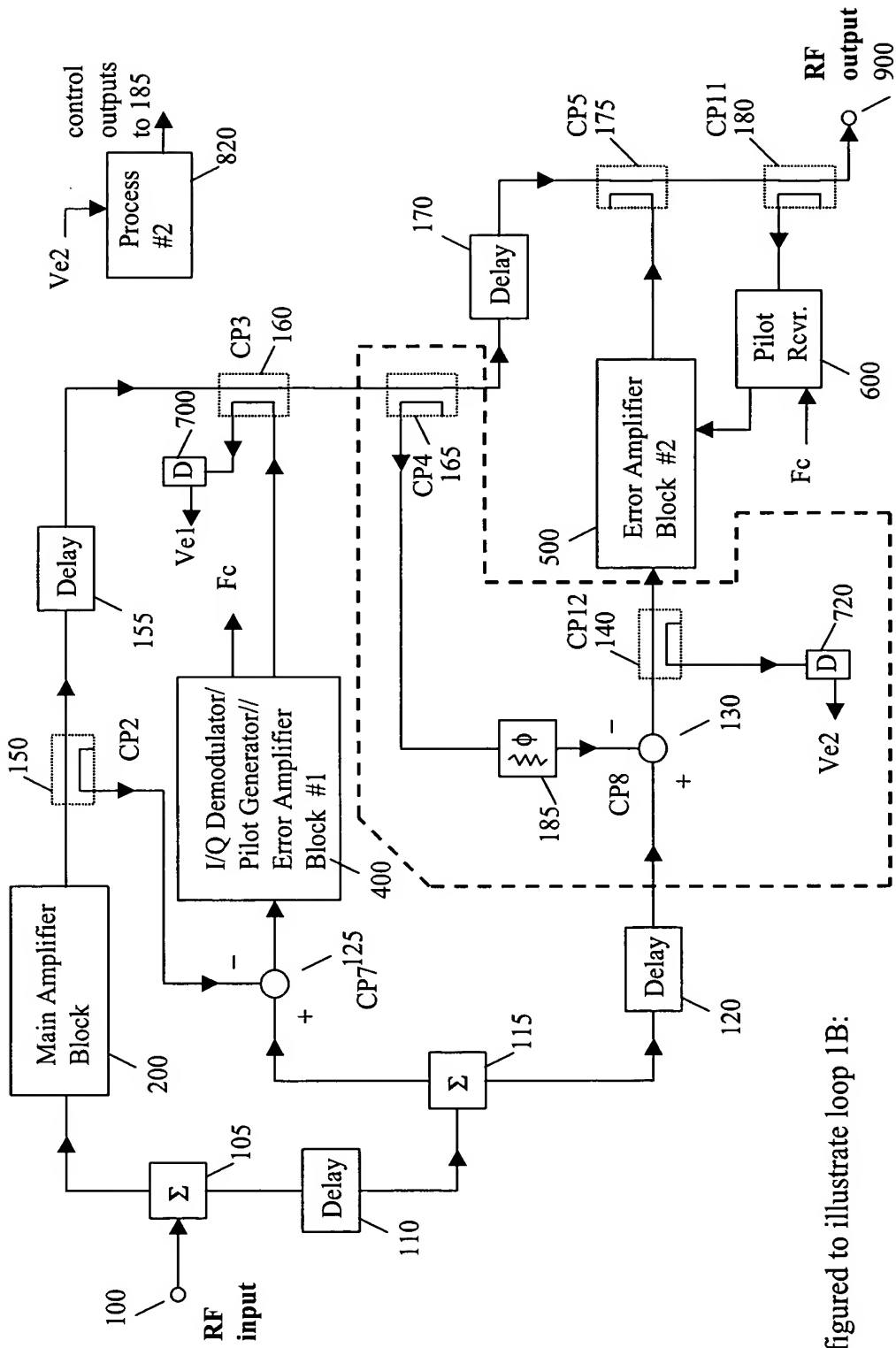


FIG. 4



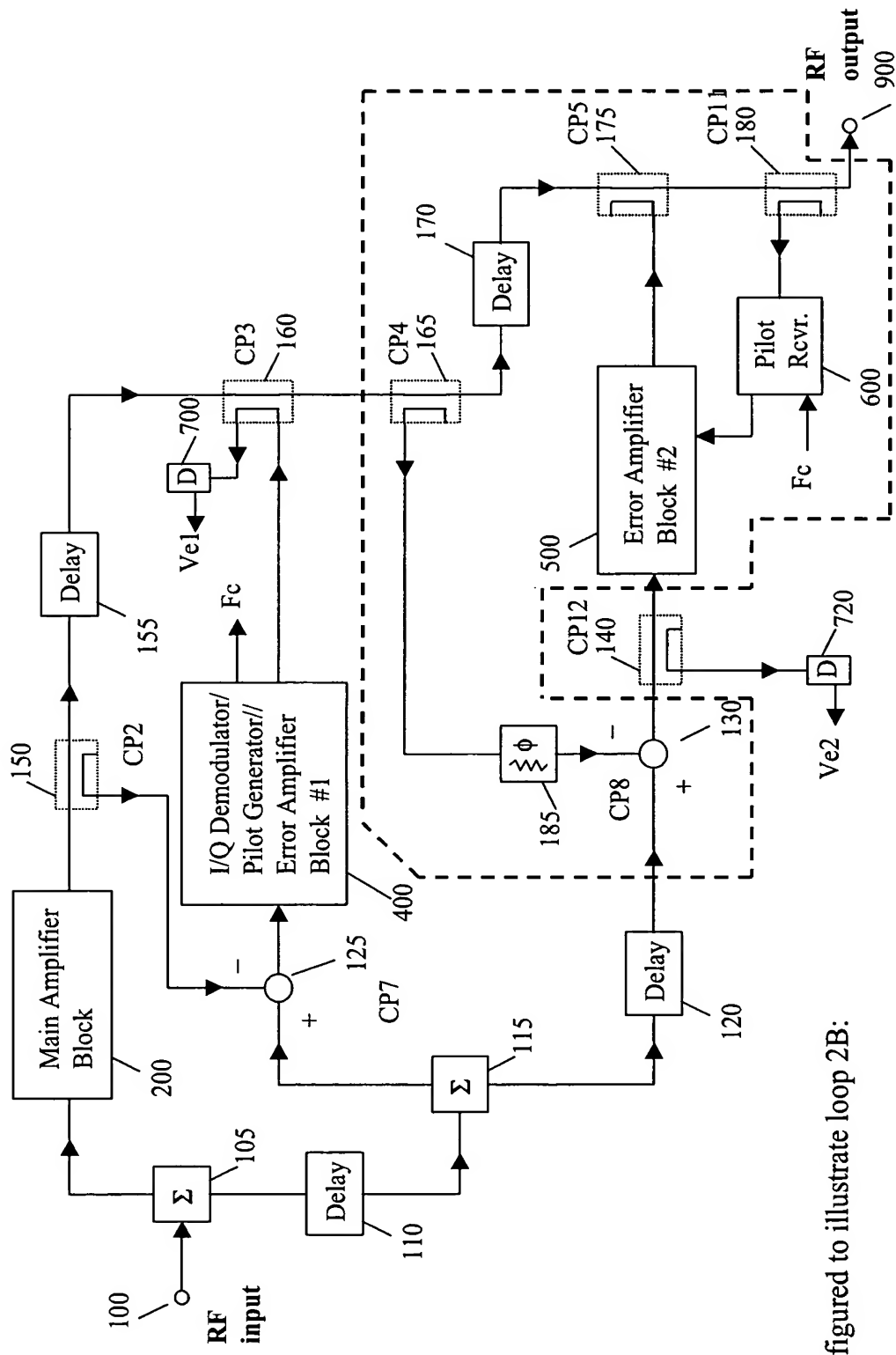
configured to illustrate loop 2A:

FIG. 5



configured to illustrate loop 1B:

FIG. 6



configured to illustrate loop 2B:

FIG. 7

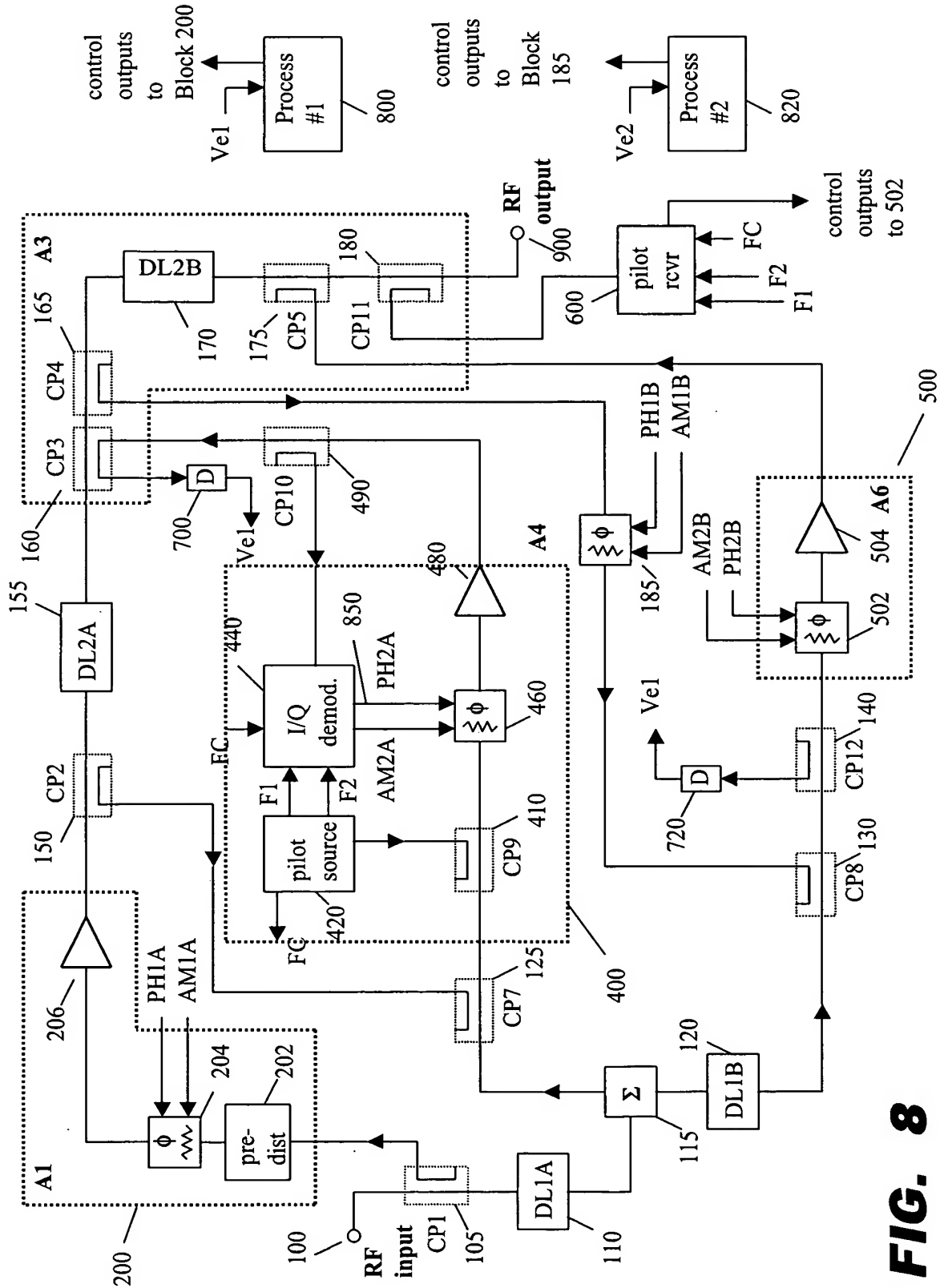


FIG. 8

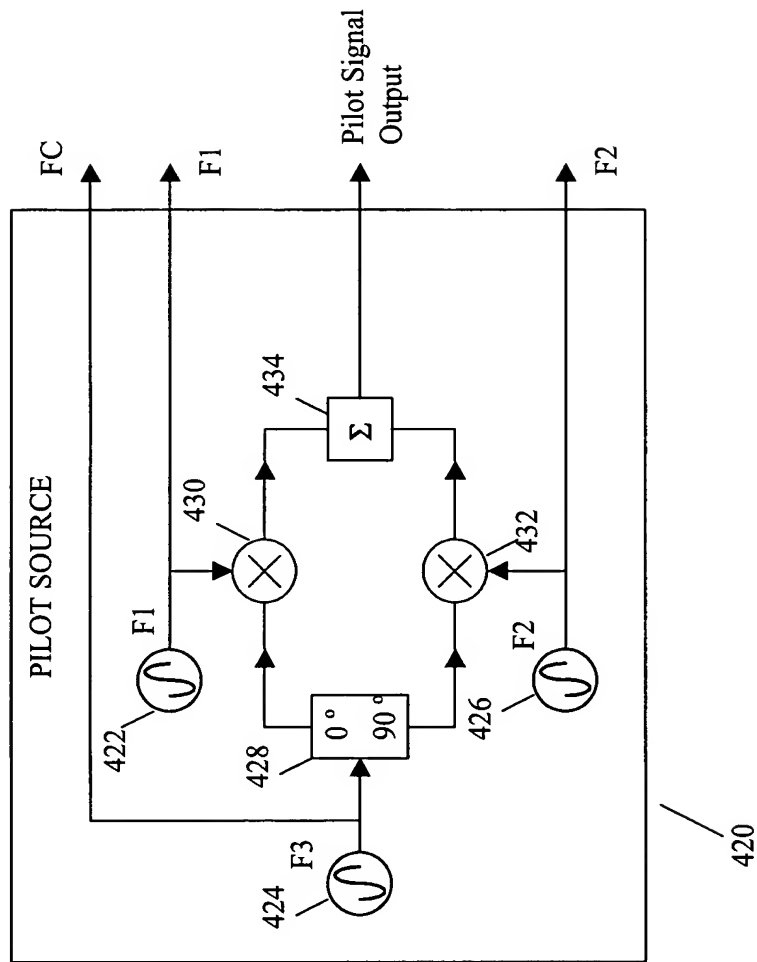
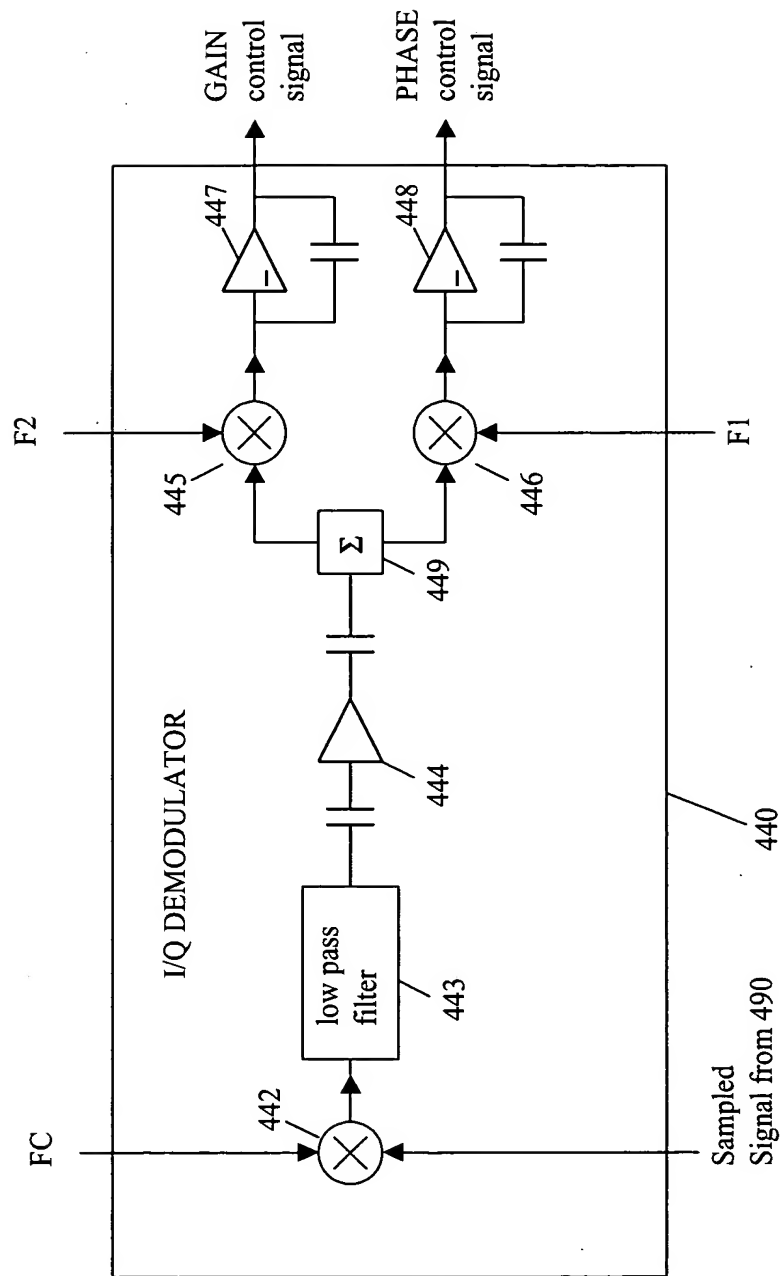


FIG. 9

**FIG. 10**

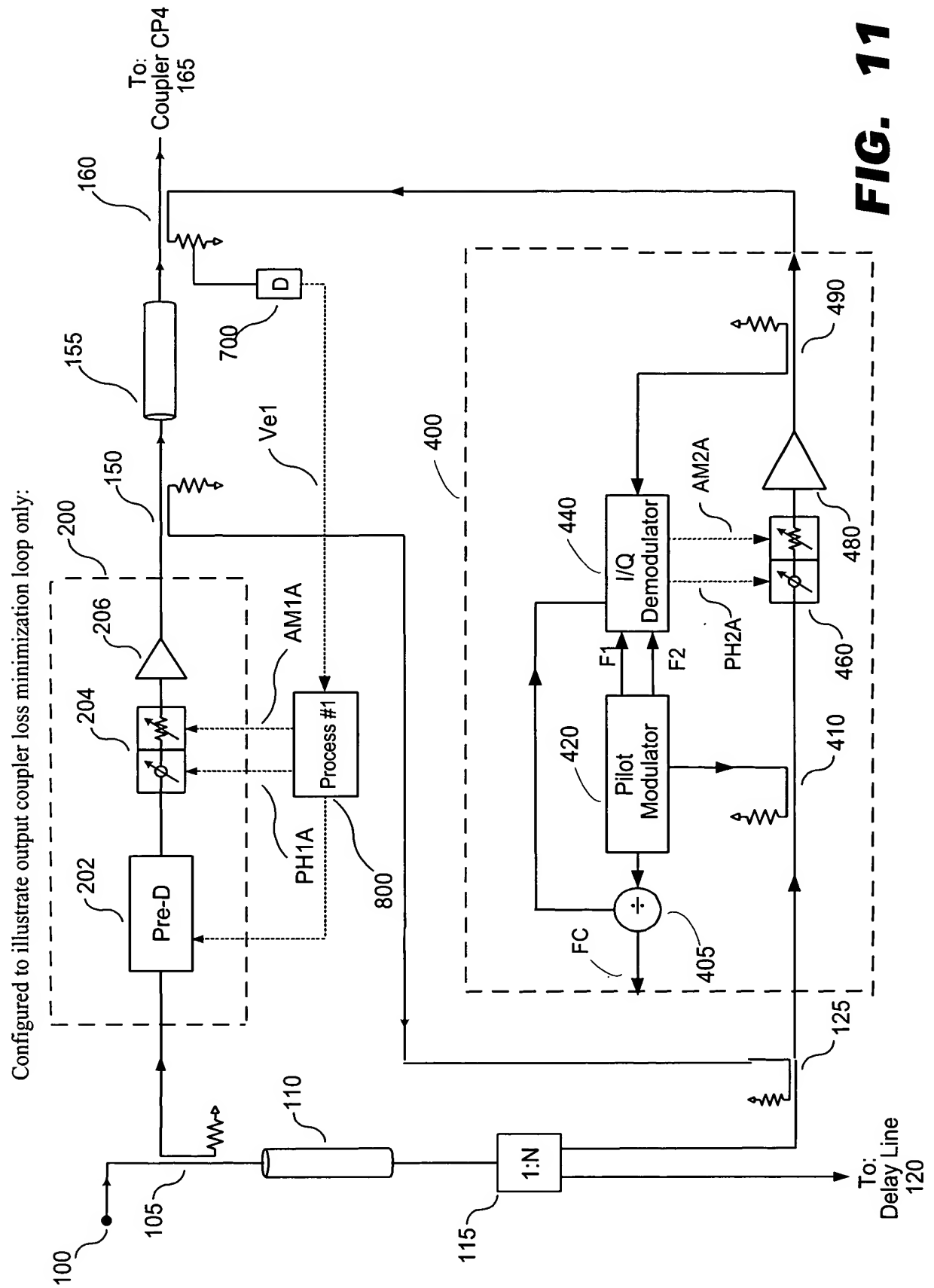


FIG. 11

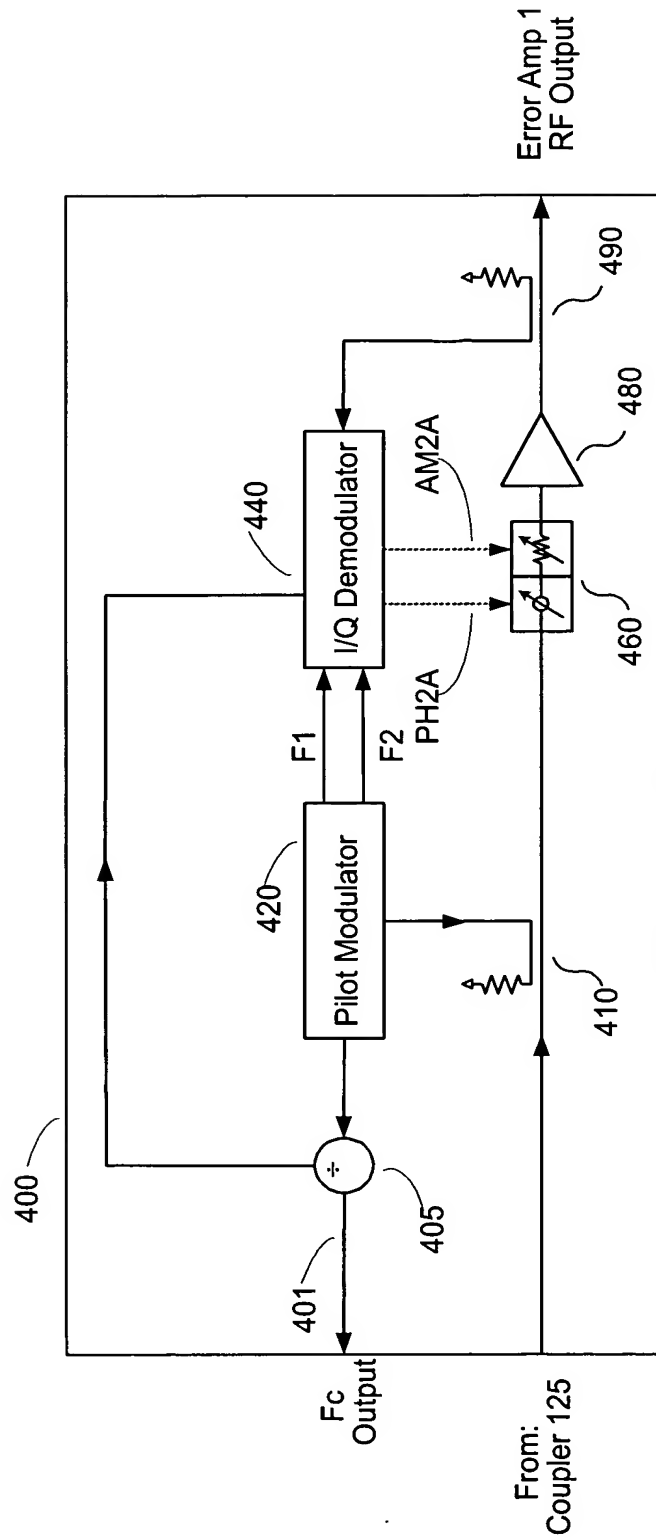
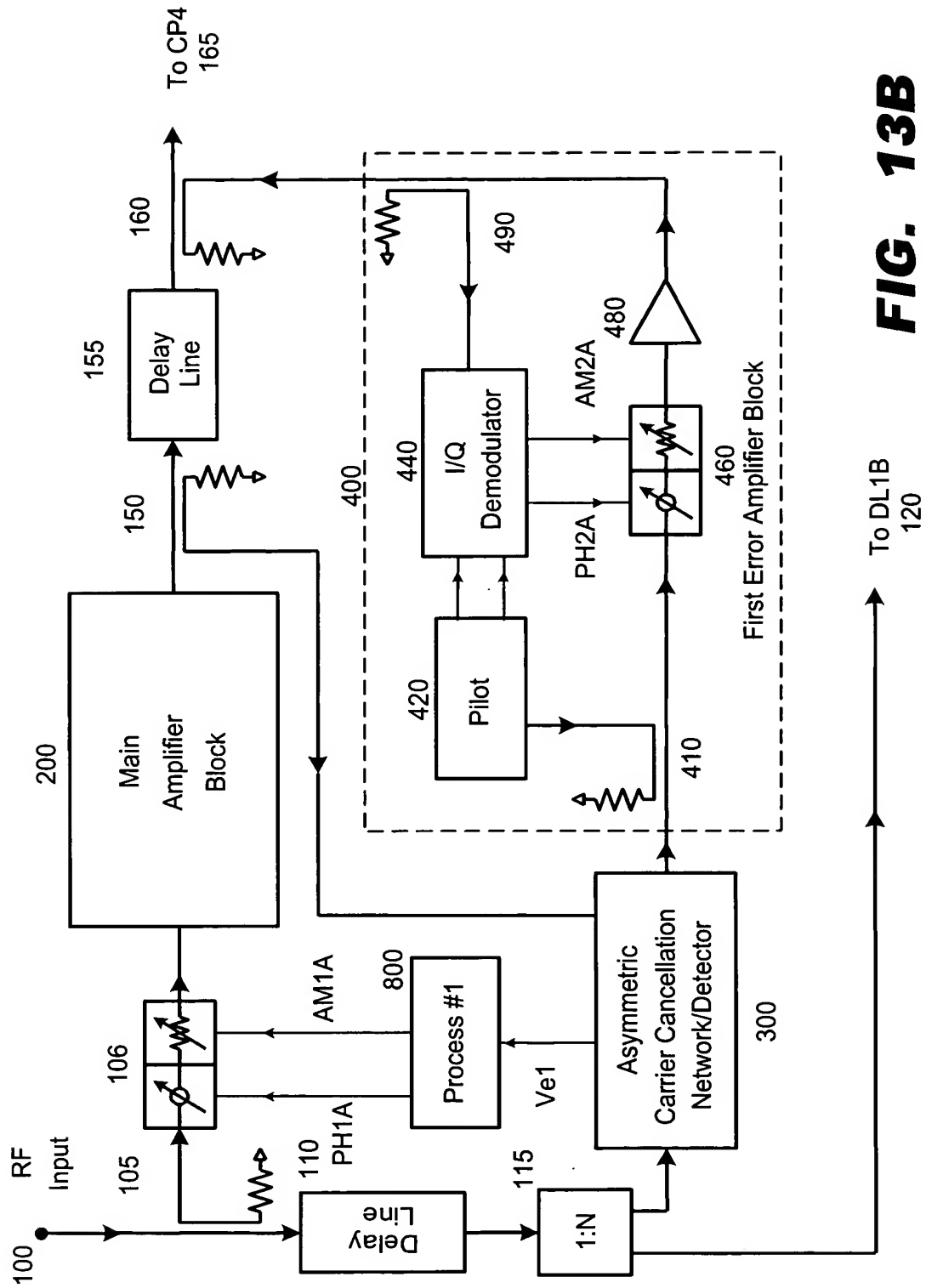


FIG. 12



FIG. 13A

**FIG. 13B**

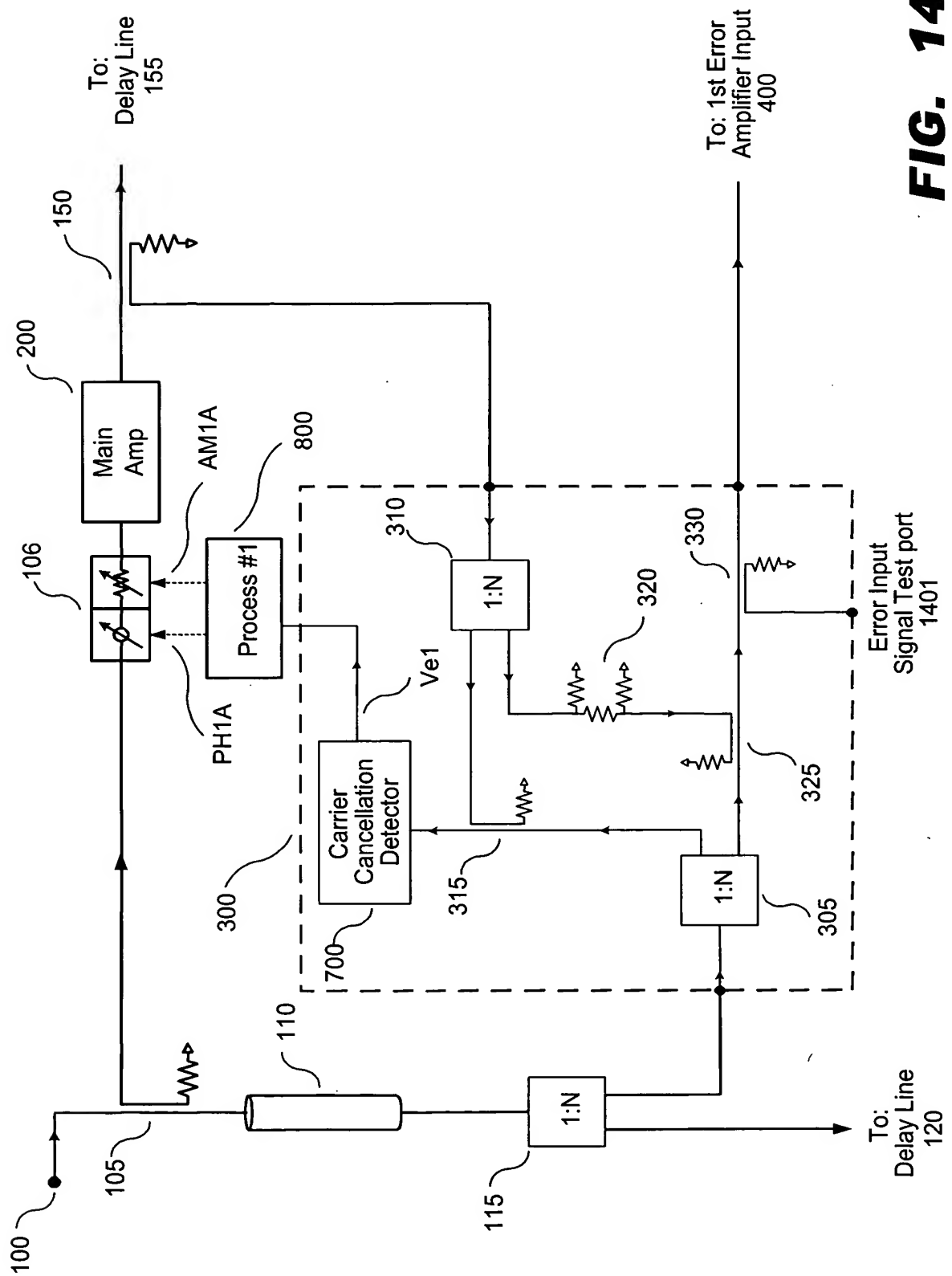


FIG. 14

1st Error Amplifier Stabilization

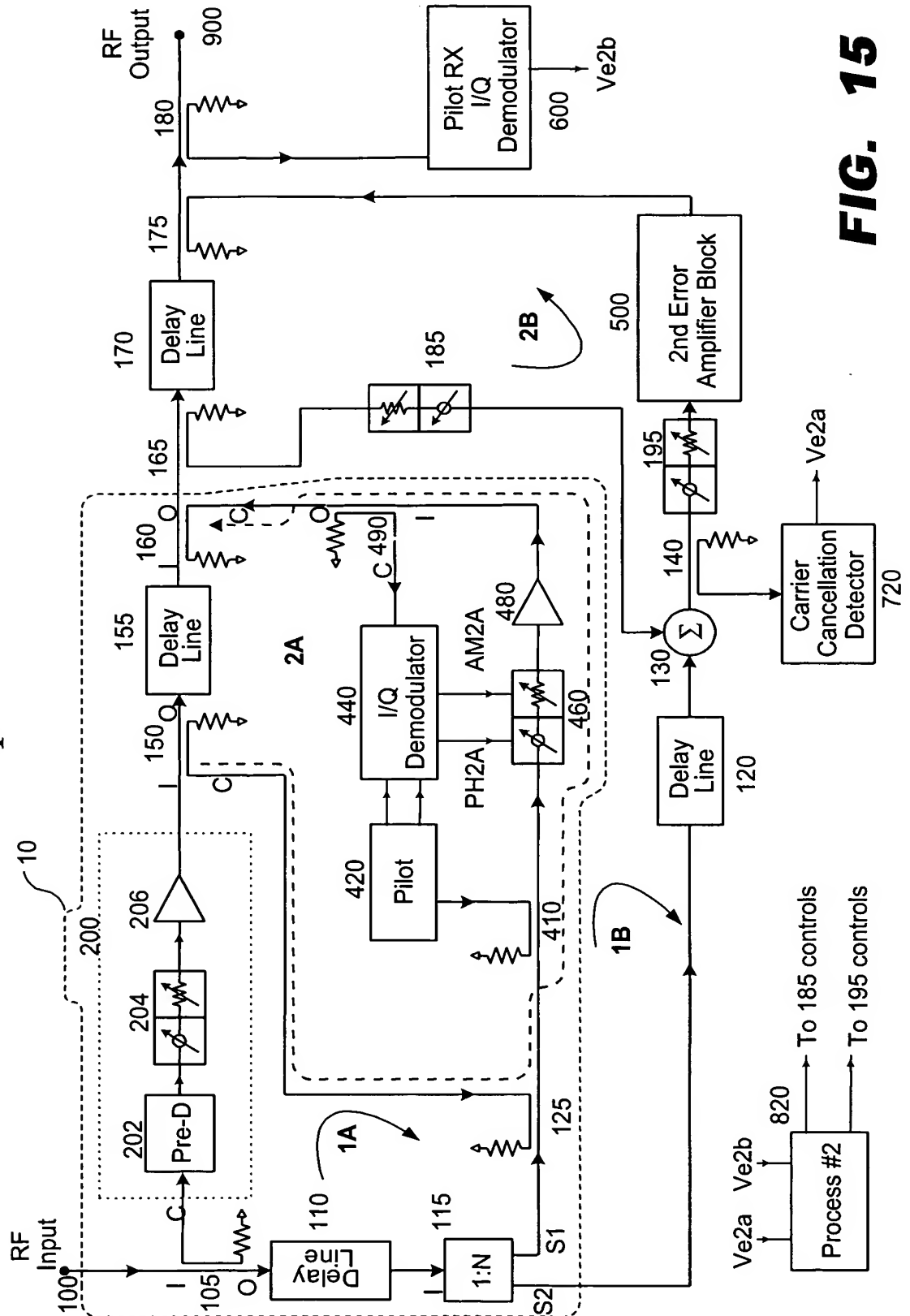


FIG. 15

Error Amplifier Stabilization

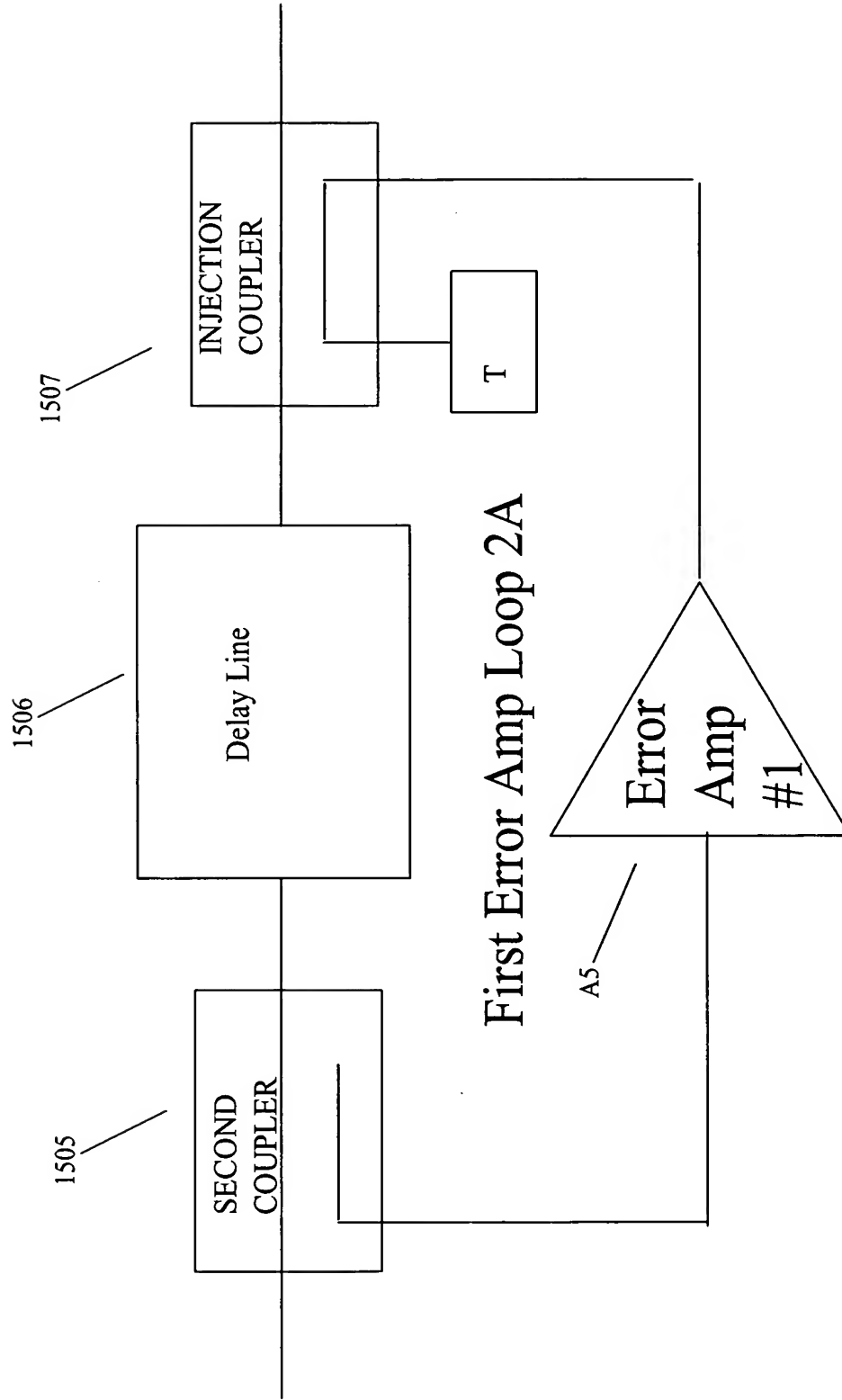


FIG. 16

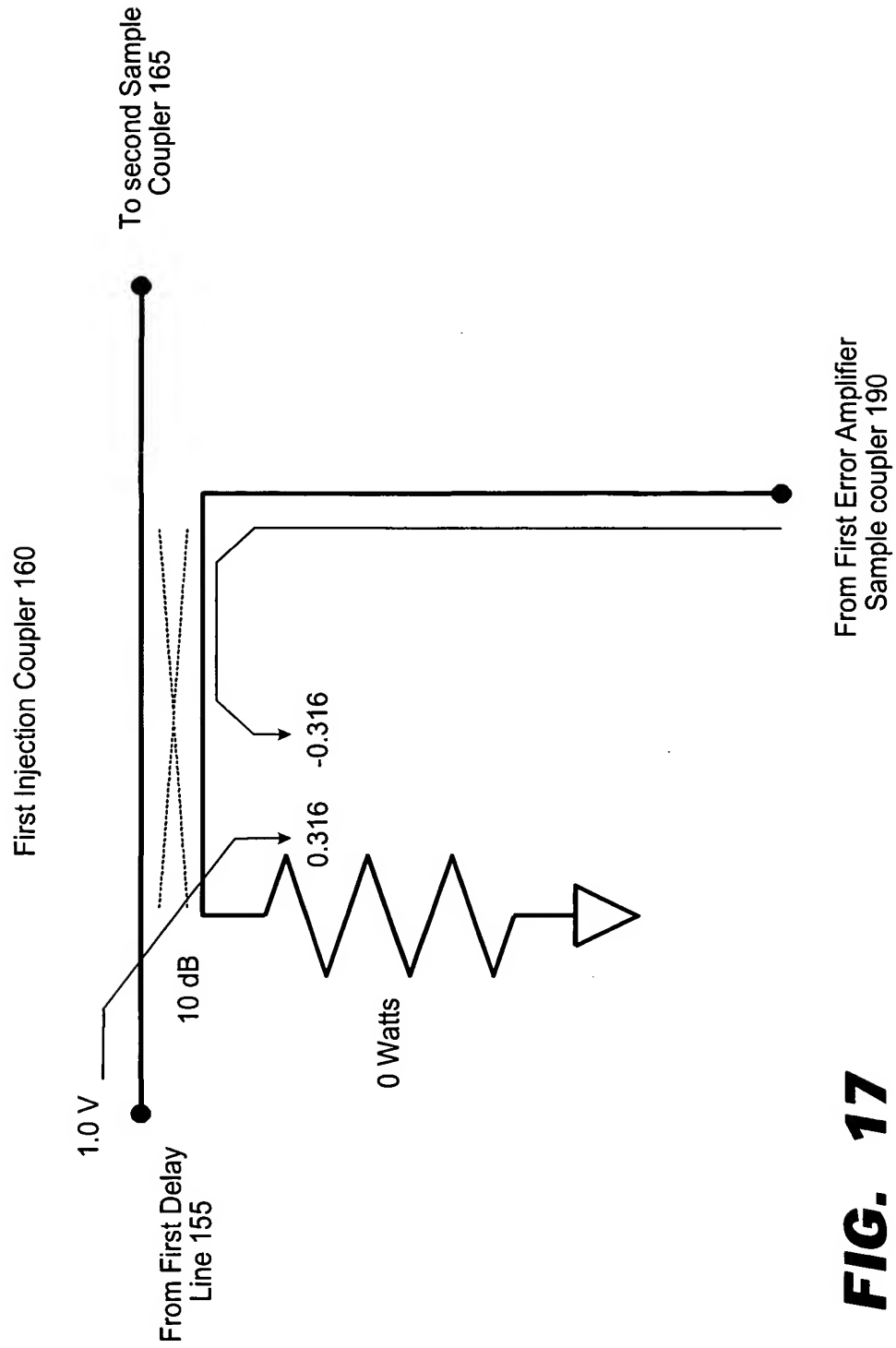


FIG. 17

Carrier Re-Injection

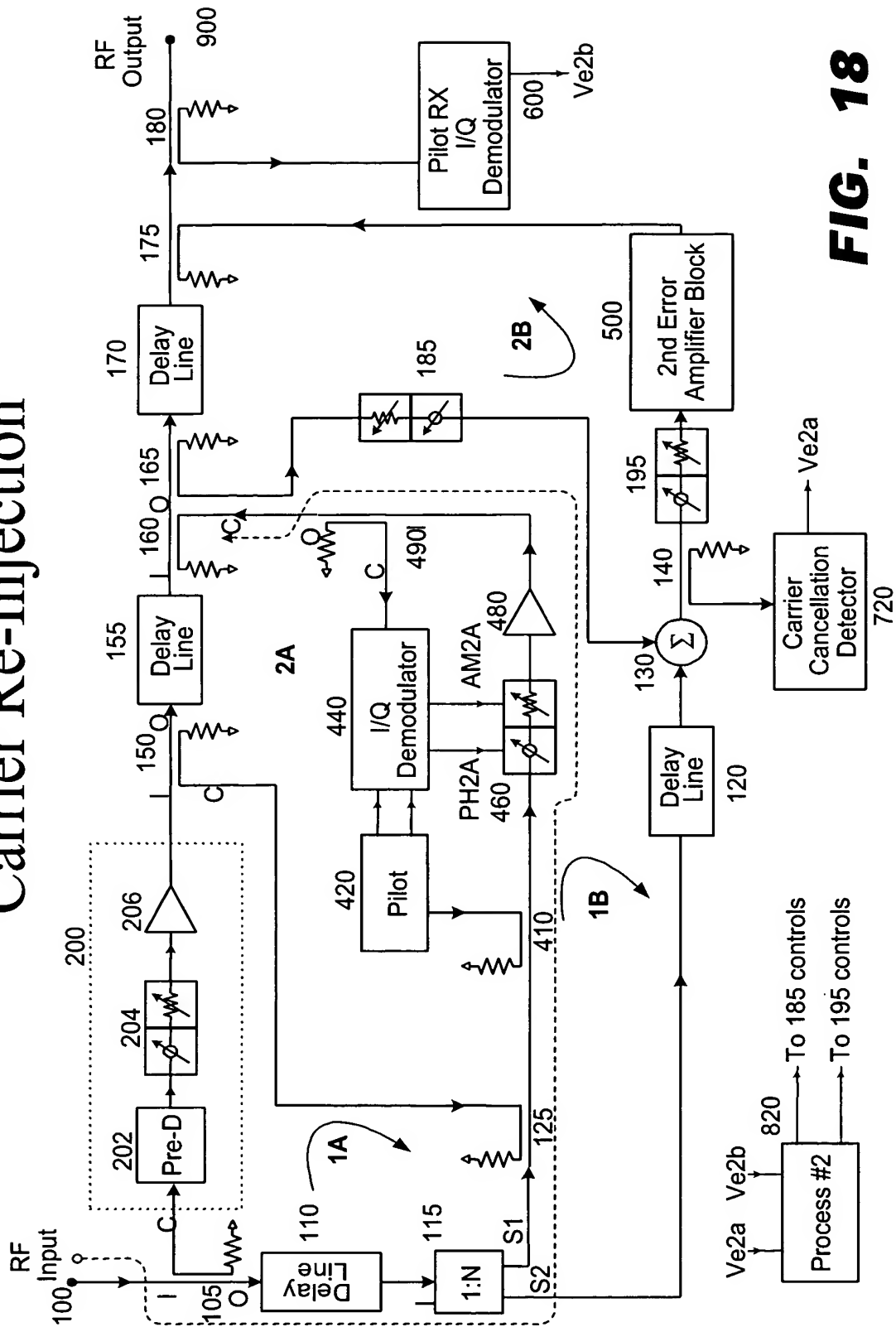


FIG. 18

Non-Overlapping Loop Adjustment

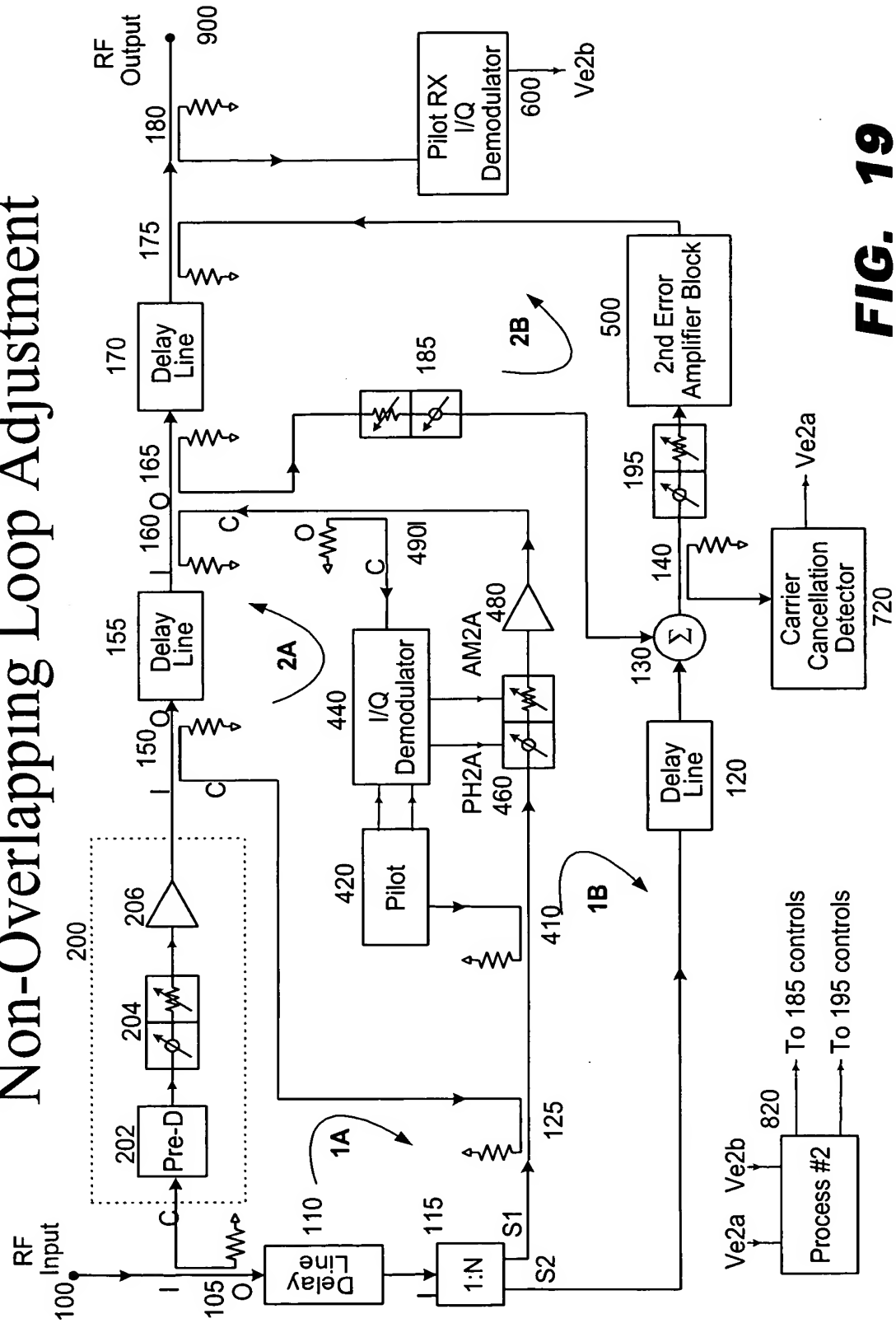


FIG. 19